Micro-transfer-printed III-V-on-Silicon C-band SOAs with 17 dB Gain

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***Abstract*—In this paper, we demonstrate the integration of a pre-fabricated semiconductor optical amplifiers on a silicon photonic integrated circuit through micro-transfer-printing. 17 dB small signal gain is obtained from the 1.35 mm long device.**

***Index Terms*—Micro-transfer-printing, heterogeneous integration, silicon photonics**

I. Introduction

Wafer-scale integration of III-V semiconductors on silicon photonic integrated circuits is of key importance to realize fully integrated complex systems-on-chip. Various approaches are currently being pursued to realize this (pick-and-place of micro-packaged lasers, flip-chip integration, die-to-wafer or wafer-to-wafer bonding, hetero-epitaxial growth), with different levels of maturity. A newcomer in the field of III-V-on-silicon photonic integrated circuits is micro-transfer-printing (μTP), illustrated in Fig. 1. μTP combines advantages of flip-chip integration (pre-processing of the III-V opto-electronic devices prior to heterogeneous integration) and wafer bonding (high throughput integration). The process starts with the definition of the III-V opto-electronic components (semiconductor optical amplifiers, lasers) on a III-V source wafer, which has the active epitaxial layer stack grown on top of a release layer (e.g. InAlAs for the InP material system). After patterning of the device and the release layer, the structures are encapsulated and the release layer is selectively removed, leaving the III-V components attached to the III-V substrate by thin tethers. With a PDMS stamp one or more III-V components can be picked up from the source wafer and printed onto a silicon photonic target wafer. Then, the encapsulation is removed and the III-V devices are electrically contacted on wafer level. This approach enables pretesting of the III-V devices on the source wafer, similar to flip-chip integration, but also massively parallel integration, similar to the die-to-wafer bonding approach. The III-V devices are micro-scale, so the silicon photonics back-end flow is not disturbed. Only a local opening to the silicon device layer is needed, similar to the flip-chip integration approach. In this paper we demonstrate the integration of C-band semiconductor optical amplifiers (SOAs) on a silicon photonic integrated circuit using micro-transfer-printing.

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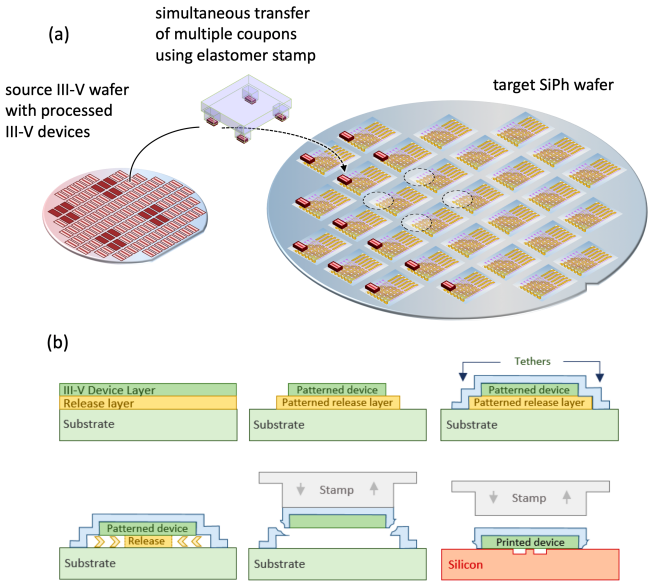

Fig. 1. Schematic of the micro-transfer-printing III-V-on-silicon heterogeneous integration process: (a) overview of wafer-level integration process; (b) zoom-in on the III-V fabrication process and printing operation.

II. SOA Design and Fabrication

A challenge in micro-transfer-printing pre-fabricated SOAs on top of silicon photonic circuits is the need of high alignment accuracy. State-of-the-art transfer printing tools have an alignment accuracy of ± 1.5 μm (3σ). This implies that the evanescently-coupled III-V-on-silicon devices in which the light has to couple from the III-V waveguide to silicon waveguide and vice versa needs to be able to cope with this misalignment. Such a taper structure was designed, based

on the method described in [1]. The silicon waveguides are defined in a 400 nm silicon layer by a 180 nm partial etch. The III-V layer structure consists of a 260 nm thick n-InP contact layer, an InAlGaAs active region with 6 quantum wells, and a 2 μm/285 nm thick p-InP/p-InGaAs cladding. The schematic of the taper and its lateral alignment tolerance is show in Fig. 2. The III-V waveguide tapers down adiabatically from 3.2 μm to 0.5 μm over 225 μm length. The silicon waveguide underneath is 3.0 μm wide over the entire length of the III-V-on-silicon structure. This way the mode resides partly in the silicon and partly in the III-V (12 percent confinement factor in the 6 quantum wells). The III-V devices are preprocesed in dense arrays on the source wafer and then micro-transfer-printed on the SOI waveguide. The pre-processing steps include classical III-V processing steps, such as formation of the SOA mesa, metallization and n-InP patterning. What is specific about the devices for micro-transfer-printing is that below the SOA epitaxial layer stack a 500 nm thick InAlAs release layer is incorporated, that is patterned and encapsulated together with the device, after which the release layer is selectively etched using an $FeCl_3$:H_2O etchant, as shown in Fig. 1b. The process flow is described in detail in [2]. After release, the devices are micro-transfer-printed on the SOI die using a DVS-BCB (60 nm) adhesive bonding agent. The top view of a micro-transfer-printed SOA is shown in Fig. 3. After the printing, the p-metal and n-metal are exposed and the devices are electrically connected.

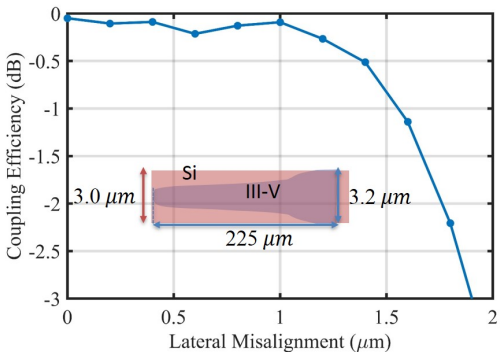

Fig. 2. Alignment tolerance of the designed III-V-on-silicon taper structure

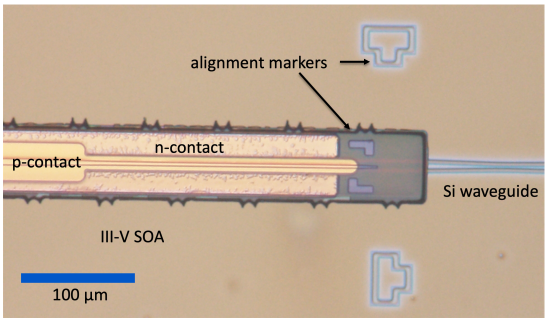

Fig. 3. Microscope image of the micro-transfer-printed SOA on the silicon waveguide circuit

III. Measurements

The III-V-on-silicon SOA was characterized on a temperature-controlled stage at 20°C. Light from a tunable laser was passed through a polarization controller and then coupled into the device under test through grating couplers (designed for TE-polarization in the C-band) and the output was recorded using an optical spectrum analyzer (OSA). The optical losses in the passive reference waveguide were characterized first using a tunable laser and OSA. The fiber angle was adjusted for the grating coupler peak wavelength to coincide with the gain peak of the gain medium. The peak output power of the SOA was measured within 1 nm around the signal wavelength to calculate the gain. This way the amplified spontaneous emission can be excluded from the gain measurements. The on-chip gain as a function of on-chip input power for three bias currents measured at 1550 nm is shown in Fig. 4. 17 dB small-signal gain at 170 mA bias current is obtained. The SOA produces an on-chip peak output power of 10 dBm for 1 dBm on-chip input power for 170 mA bias current (456 mW power consumption).

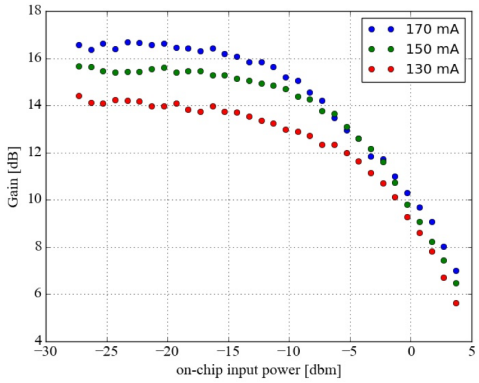

Fig. 4. III-V-on-Si SOA on-chip gain as a function of on-chip input power for three different SOA bias currents at 1550 nm

IV. Conclusion

In this paper we demonstrated a III-V-on-silicon SOA with 17 dB small signal gain using micro-transfer-printing of pre-fabricated III-V semiconductor optical amplifiers on a silicon waveguide circuit. This demonstration showcases the great potential that the micro-tansfer-printing technique has for the realization of III-V-on-silicon photonic integrated circuits.

References

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